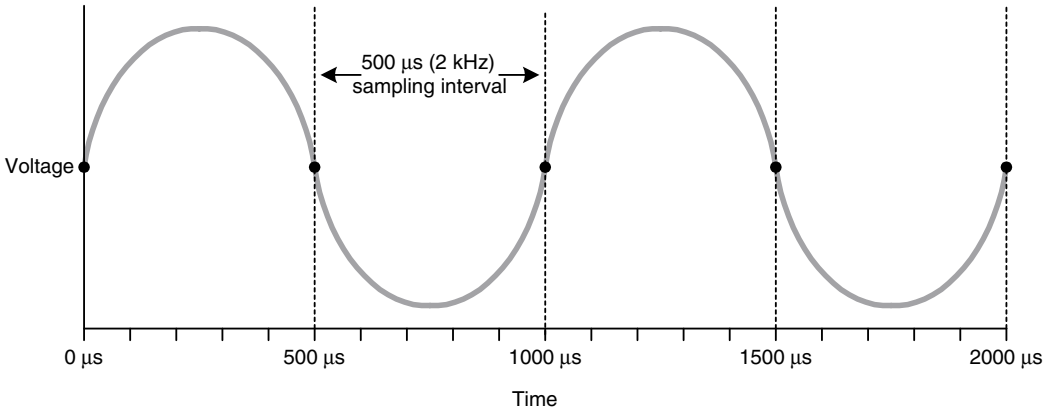

FIGURE 15.6 1-kHz sine wave sampled at the Nyquist frequency.

When a data conversion circuit is operated above the Nyquist frequency, *aliasing* develops, which distorts the information content of a signal. Aliasing occurs when a high-frequency signal is made to appear as a low-frequency signal as a result of inadequate sampling. Assume that a 1-kHz input is expected and a 3-kHz sampling rate is designed to satisfy the Nyquist theorem with some margin. For some reason, a 2-kHz signal enters the system. Figure 15.7 shows how this signal might be sampled. The 333 µs sampling interval is too slow to capture each 250 µs high and low phase of the 2-kHz signal. As a result, the samples convey information that is drastically different from the input. Instead of 2 kHz, the high-low-high interval of the samples indicates a 1-kHz signal! This 1-kHz aliased signal is the difference between the sampling rate and the actual signal frequency.

Aliasing applies to the analog-to-digital conversion process. When converting from digital to analog, the DAC is inherently self-limited by the sampling rate such that the highest frequency it can generate is half the sampling rate, or the Nyquist frequency. This behavior would result if consecu-

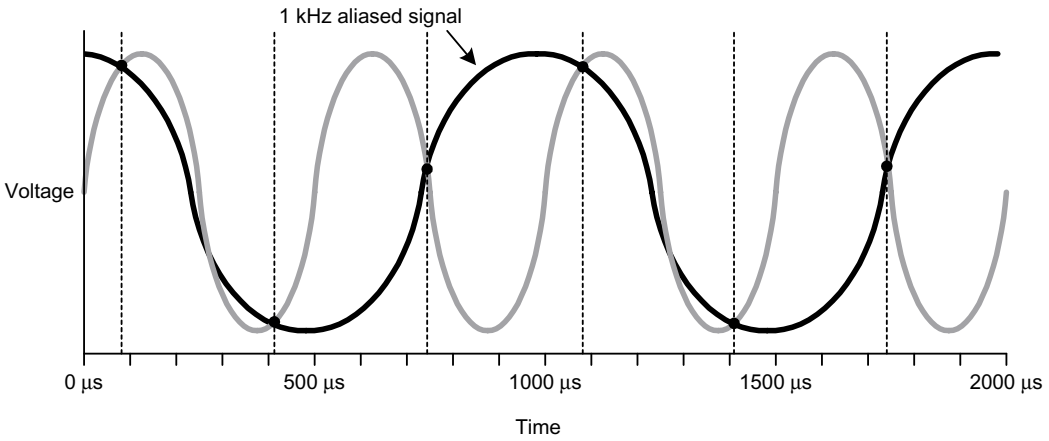

FIGURE 15.7 2-kHz sine wave sampled at 3 kHz with aliasing to 1 kHz.

tive samples alternated voltage levels about some DC level. A suitable lowpass filter on the DAC's output would remove the high-frequency edges and leave behind a sine wave of half the sampling frequency as shown in Fig. 15.8.

Lowpass filtering is a critical part of the data conversion process, because it removes unwanted sampling artifacts at DAC outputs and prevents aliasing at ADC inputs. The necessary slope of the filter's roll-off depends on how close unwanted high frequencies are to the Nyquist frequency.

15.3 ADC CIRCUITS

ADCs are available in a wide range of sampling rates and resolutions. The basic internal architecture of an ADC is straightforward, as shown in Fig. 15.9. A *sample and hold* (S/H) circuit captures a snapshot of the analog input signal so that the conversion circuit can work with a fixed sample over the conversion interval, which can be as long as the sampling interval. An ideal S/H circuit captures the input signal in zero time so that a true instantaneous sample is taken. In reality, the small capacitor that is used to hold the sample during conversion takes a finite time to charge through a finite switch resistance to the same voltage as the input. Once the conversion circuit maps the captured voltage to a digital sample, the digital interface conveys this information to the digital processor. ADC interfaces are available in both serial and parallel configurations.

A variety of basic analog-to-digital conversion circuits are used, based on the desired sampling rate and resolution. Three of the most common are *flash*, *successive-approximation*, and *sigma-delta*. A flash ADC, shown in Fig. 15.10, consists of a bank of parallel comparators, each fed by a unique incremental reference voltage. Each comparator's output represents one of the $2^N - 1$ possible outputs of the ADC. By process of elimination, the lowest quantum is not represented by a comparator, because it is implied if none of the comparators are at logic 1. Therefore, a 12-bit flash ADC

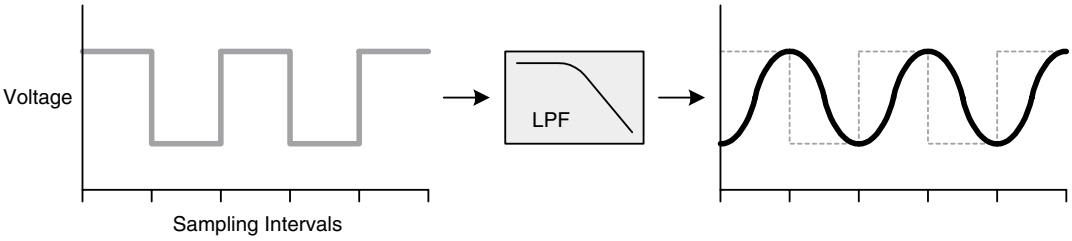

FIGURE 15.8 Maximum frequency output of the DAC.

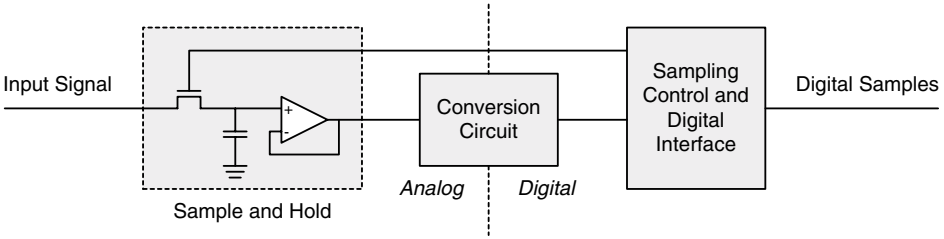

FIGURE 15.9 Basic ADC architecture.